A Defect-Detection Graph-Based Methodology for Cell-Aware Model Generation

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As modern Integrated Circuits (ICs) incorporate increasingly smaller transistors, the occurrence of manufacturing defects within standard cells (intra-cell defects) has risen. Detecting and localizing these defects is essential for ensuring a rapid yield ramp-up and maintaining a low-test escape rate. To address intra-cell defects, Cell-Aware (CA) methodology was introduced, but it relies on time-consuming analog SPICE simulations for standard cell characterization. This paper introduces Transistor Undetectable Defect Eliminator (TrUnDeL), a graph-based methodology designed to expedite the CA model generation process. TrUnDeL identifies undetectable defects for each stimulus applied to cell inputs, excluding them from required analog simulations. TrUnDeL was tested on two FD-SOI standard cell libraries (P28 and C28) from STMicroelectronics. The results show that, for combinational cells, the CA model generation process time was reduced by a factor of three compared to standard analog-based methods without compromising accuracy. To efficiently address sequential cells, modifications to the classical TrUnDeL flow were implemented, resulting in a 30% reduction in CA model generation time for sequential cells, again without compromising accuracy. TrUnDeL was also tested on a 4x4 SRAM case study, maintaining accuracy across all memory modules. Finally, the paper introduces Layout-TrUnDeL for addressing layout defects, proving effective on 8 test-case cells without misclassification